WHAT IS CLAIMED IS:

1. An input buffer circuit comprising:

a first inverting switch connected to a first input voltage and outputting a self bias signal;

a second inverting switch connected to a second input voltage and an output signal; and

a gain control unit having a feedback loop for gain control and responding to the self bias signal and the output signal.

2. The input buffer circuit of claim 1, wherein the gain control unit comprises:

a first PMOS transistor having a source connected to a first node, a drain connected to the self bias signal and a gate connected to the output signal;

a first NMOS transistor having a source connected to a second node, a drain connected to the self bias signal and a gate connected to the output signal;

a second PMOS transistor having a source connected to the first node, a drain connected to the output signal and a gate connected to the self bias signal; and

a second NMOS transistor having a source connected to the second node, a drain connected to the output signal and a gate connected to the self bias signal.

3. The input buffer circuit according to claim 2, wherein the gain control unit further comprises:

a third PMOS transistor having a source connected to the first node, a gate and a drain connected to the self bias signal; and

a third NMOS transistor having a source connected to the second node, a gate and a drain connected to the self bias signal.

4. An input buffer circuit comprising:

a first inverting switch connected to a first input voltage and outputting a self bias signal;

a second inverting switch connected to a second input voltage and outputting a output signal;

a gain control unit having a feedback loop for gain control responsive to the self bias signal and the output signal; and

a current controlling circuit that supplies current to the first inverting switch, the second inverting switch and the gain control unit and sinks current from the first inverting switch, the second inverting switch and the gain control unit, the current controlling circuit responding to the self bias signal.

5. The input buffer circuit of claim 4, wherein the gain control unit comprises:

a first PMOS transistor having a source connected to a first node, a drain connected to the self bias signal and a gate connected to the output signal;

a first NMOS transistor having a source connected to a second node, a drain connected to the self bias signal and a gate connected to the output signal;

a second PMOS transistor having a source connected to the first node, a drain connected to the output signal and a gate connected to the self bias signal; and

a second NMOS transistor having a source connected to the second node, a drain connected to the output signal and a gate connected to the self bias signal.

6. The input buffer circuit according to claim 5, wherein gain control unit further comprises:

a third PMOS transistor having a source connected to the first node, a gate and a drain connected to the self bias signal;

a third NMOS transistor having a source connected to the second node, a gate and a drain connected to the self bias signal.

7. The input buffer circuit of claim 5, wherein the current controlling circuit comprises:

a third PMOS transistor having a source connected to the first node, a drain connected to the gain control unit to supply current and a gate connected to the self bias signal; and

a third NMOS transistor having a source connected to the second node, a drain connected to the gain control unit to sink current and a gate connected to self bias signal.

8. An input buffer circuit comprising:

a first inverting switch connected to a first input voltage and outputting a self bias signal;

a second inverting switch connected to a second input voltage and outputting a output signal;

a gain control unit having a feedback loop for gain control responsive to the self bias signal and the output signal; and

a swing width control circuit connected to a feedback signal that is inverted by the output signal.

9. The input buffer circuit of claim 8, wherein the gain control unit comprises:

a first PMOS transistor having a source connected to a first node, a drain connected to the self bias signal and a gate connected to the output signal;

a first NMOS transistor having a source connected to a second node, a drain connected to the self bias signal and a gate connected to the output signal;

a second PMOS transistor having a source connected to the first node, a drain connected to the output signal and a gate connected to the self bias signal; and

a second NMOS transistor having a source connected to the second node, a drain connected to the output signal and a gate connected to the self bias signal.

10. The input buffer circuit of claim 9, wherein the gain control unit further comprises:

a third PMOS transistor having a source connected to the first node, a gate and a drain connected to the self bias signal;

a third NMOS transistor having a source connected to the second node, a gate and a drain connected to the self bias signal.

11. The input buffer of claim 8, wherein the swing width control circuit comprises:

an NMOS transistor having a source connected to the output signal, a drain connected to the current controlling circuit and a gate connected to the feedback signal; and

a PMOS transistor having a source connected to the output signal, a drain connected to the current controlling circuit and a gate connected to the feedback signal.

12. An input buffer circuit comprising:

a first inverting switch connected to a first input voltage and outputting a self bias signal;

a second inverting switch connected to a second input voltage and outputting an output signal;

a gain control unit having a feedback loop for gain control responsive to the self bias signal and the output signal;

a current controlling circuit that supplies current to the first inverting switch, the second inverting switch and the gain control unit and sinks current from the first inverting switch, the second inverting switch and the gain control unit, the current controlling circuit responding to the self bias signal; and

a swing width control circuit connected to a feedback signal that is inverted by the output signal.